PowerMOS transistor Logic level FET

PHX3055L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope. The device features high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

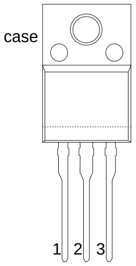
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	9.4	A
P_{tot}	Total power dissipation	28	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.18	Ω

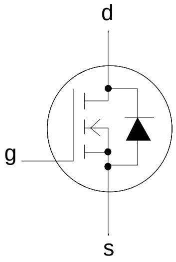
PINNING - SOT186A

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	T_{hs} = 25 ˚C; V_{GS} = 10 V	-	9.4	A
		T_{hs} = 100 ˚C; V_{GS} = 10 V	-	5.9	A
I_{DM}	Pulsed drain current	T_{hs} = 25 ˚C	-	26	A
P_D	Total dissipation	T_{hs} = 25 ˚C	-	28	W
$\Delta P_D/\Delta T_{hs}$	Linear derating factor	T_{hs} > 25 ˚C	-	0.22	W/K
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Non-repetitive gate source voltage	$t_p \leq 50\mu s$	-	± 20	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	25	mJ
I_{AS}	Peak avalanche current	$V_{DD} \leq 50$ V; starting T_j = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	6	A
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	˚C

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heat sink.		-	-	4.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; I_D = 0.25 mA	-	0.06	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 6 A	-	0.13	0.18	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 0.25 mA	1.0	1.5	2.0	V
g_{fs}	Forward transconductance	V_{DS} = 50 V; I_D = 6 A	3.5	5.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0 V	-	0.1	25	µA
		V_{DS} = 48 V; V_{GS} = 0 V; T_j = 150 ˚C	-	1	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 10 A; V_{DD} = 48 V; V_{GS} = 10 V	-	7.5	10	nC
Q_{gs}	Gate-source charge		-	1.9	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.5	7	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V; I_D = 10 A;	-	12	-	ns
t_r	Turn-on rise time	R_G = 24 Ω; R_D = 2.7 Ω	-	105	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
t_f	Turn-off fall time		-	35	-	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	290	-	pF
C_{oss}	Output capacitance		-	103	-	pF
C_{rss}	Feedback capacitance		-	40	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	9.4	A
I_{SM}	Pulsed source current (body diode)		-	-	48	A
V_{SD}	Diode forward voltage	I_S = 10 A; V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_S = 10 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	40	-	ns
Q_{rr}	Reverse recovery charge		-	0.1	-	µC

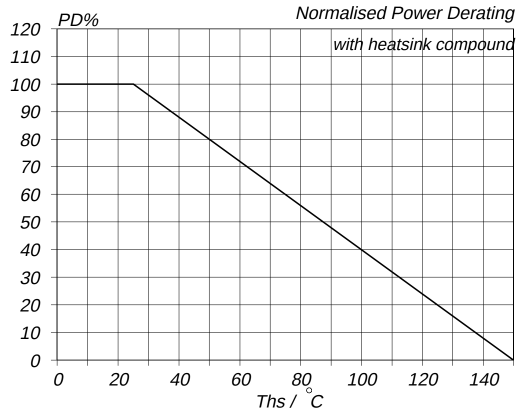


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ^{\circ}C} = f(T_{hs})$

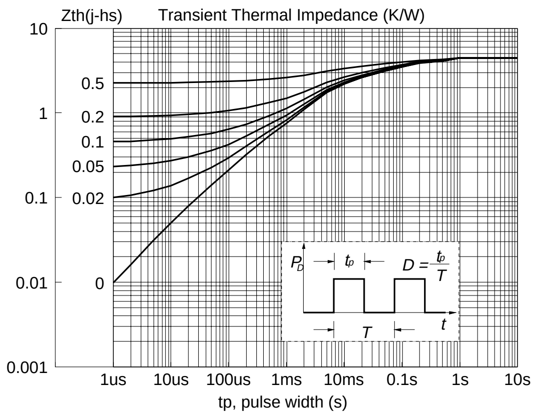


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}hs} = f(t)$; parameter $D = t_p/T$

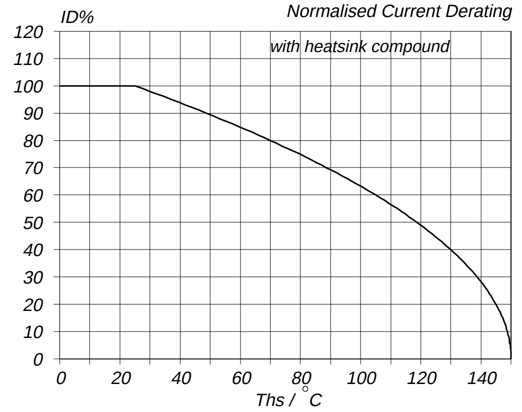


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ^{\circ}C} = f(T_{hs})$; conditions: $V_{GS} \geq 10\ V$

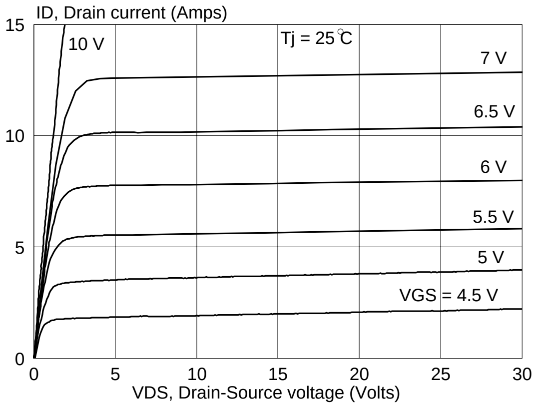


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

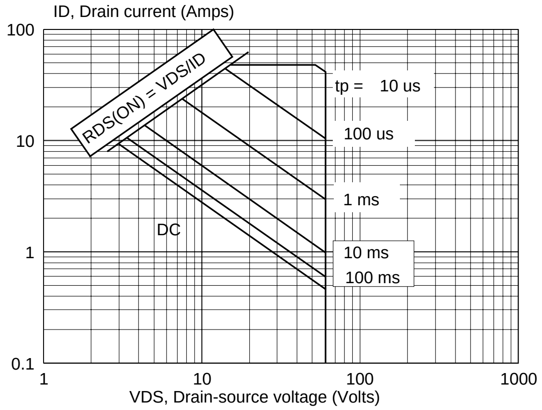


Fig.3. Safe operating area. T_{hs} = 25 ˚C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

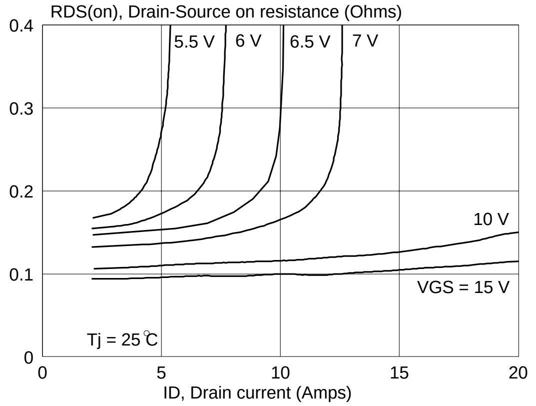


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

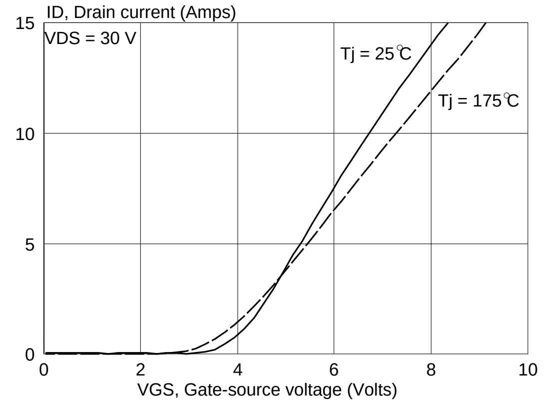


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

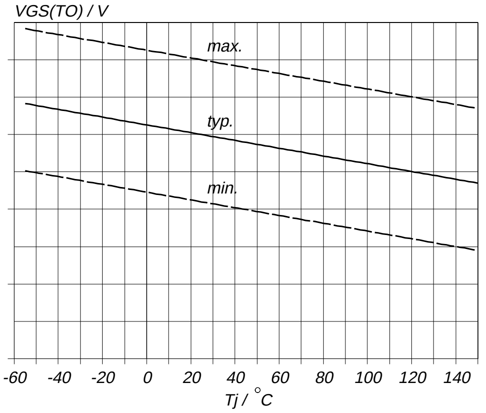


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 0.25$ mA; $V_{DS} = V_{GS}$

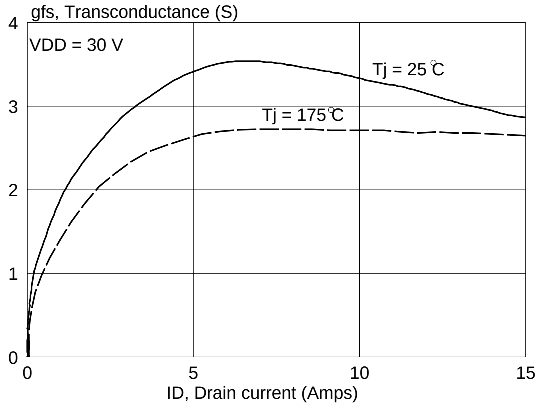


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

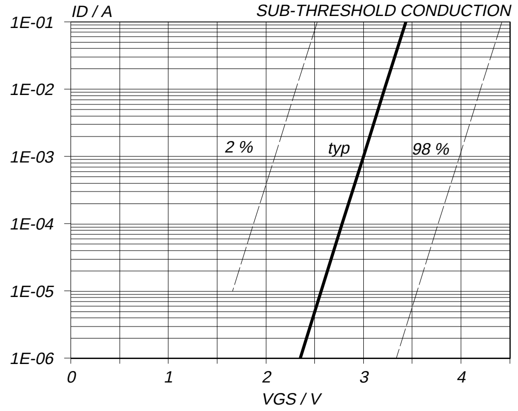


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

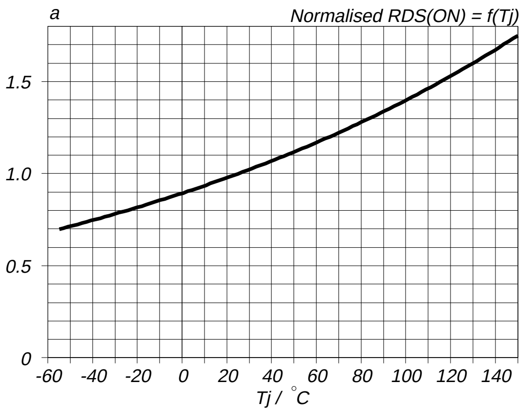


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^\circ C} = f(T_j)$; $I_D = 10$ A; $V_{GS} = 10$ V

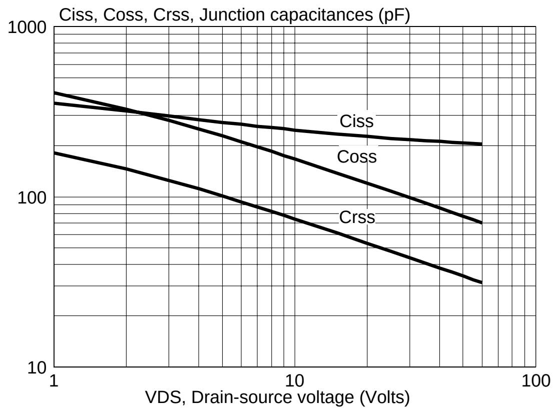


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

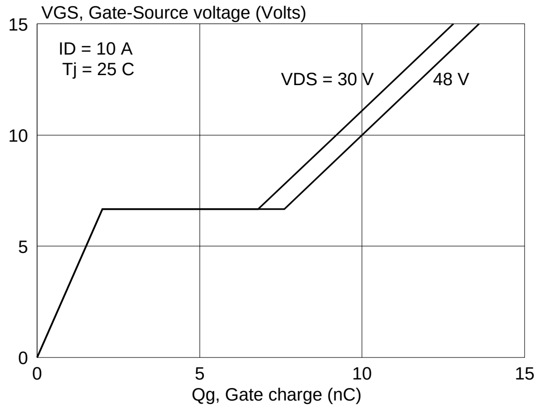


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

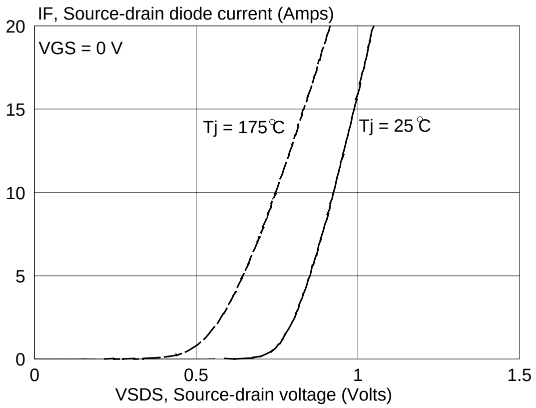


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

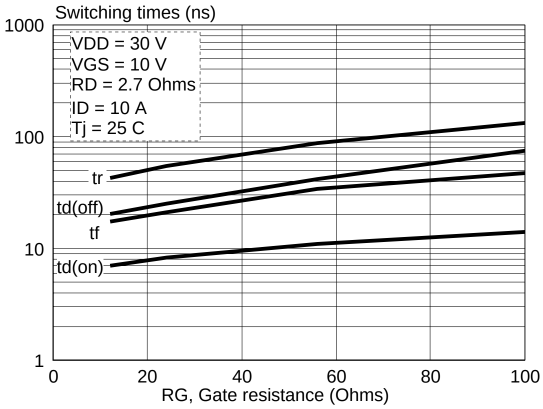


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

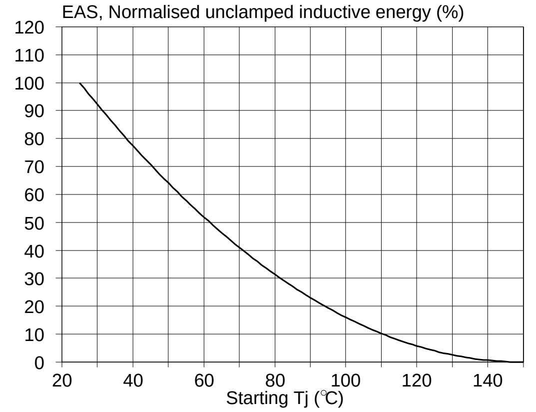


Fig.17. Normalised unclamped inductive energy.
$E_{AS}\% = f(T_j)$

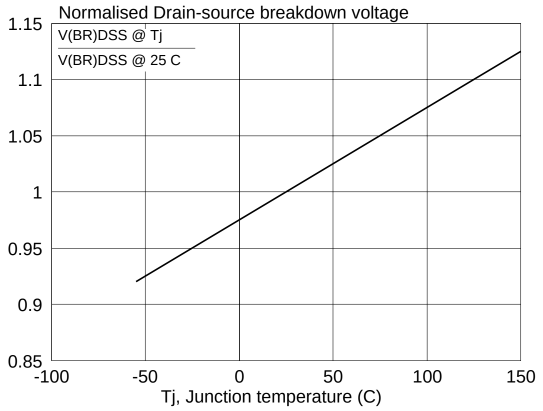


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

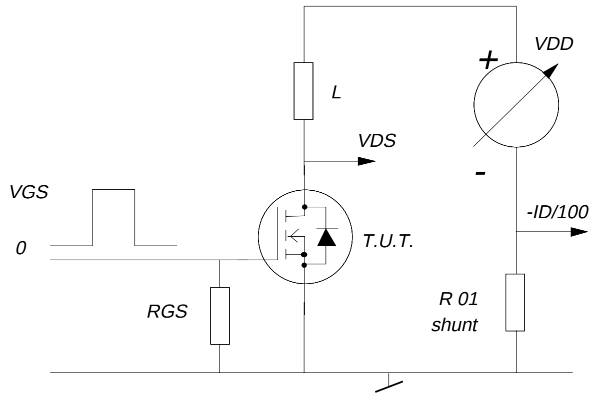


Fig.18. Unclamped inductive test circuit.
$E_{AS} = 0.5 \cdot L I_D^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS} - V_{DD})$

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

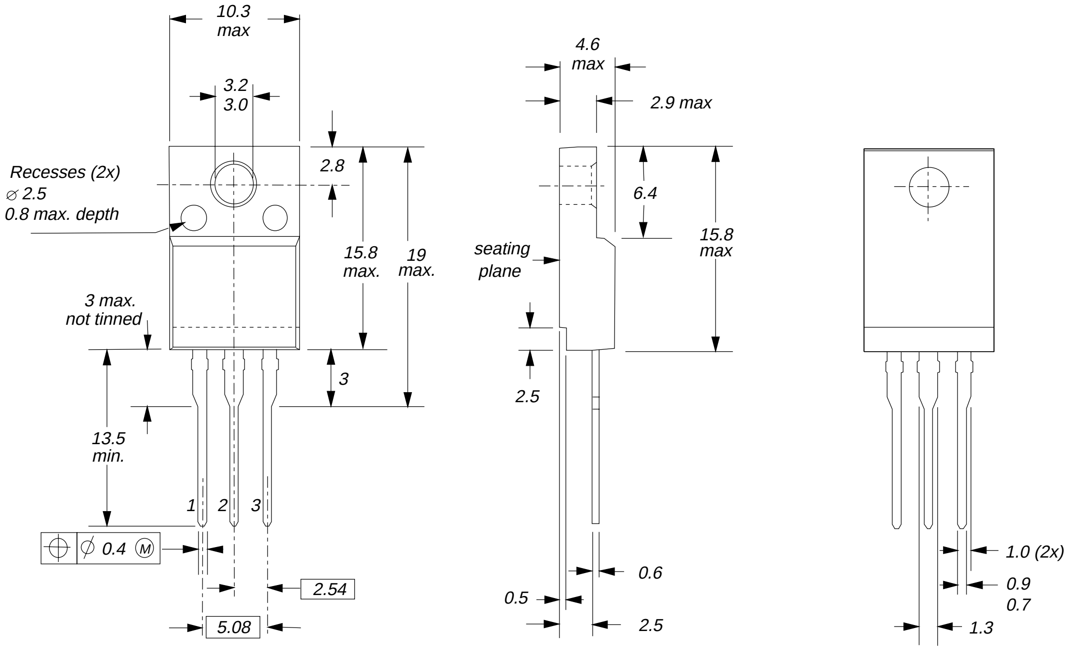


Fig.19. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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